

Integration of Nanophotonic Devices for On-Chip Optical Interconnects

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Abstract

Compact germanium waveguide photodetector with 40Gbps bandwidth and 0.4A/W responsivity is demonstrated. High-quality Ge-on-insulator single-crystalline layer was monolithically integrated into front-end CMOS process by lateral seeded crystallization.

As the number of cores in a microprocessor increases, the communication bandwidth provided by electrical interconnects becomes the bottleneck which reduces processor performance. Optical interconnects are attractive solutions for achieving communication bandwidth well beyond terabit-per-second for high-performance multi-core microprocessors. Specifically, deeply scaled silicon nanophotonic devices have shown great promise as components for on-chip optical links.

Due to its transparency in the infrared wavelength range, silicon has become a desirable material for guiding light. The high index-contrast between silicon and air or oxide results in high mode confinement, thus enabling very compact waveguide dimensions. Furthermore, silicon provides the opportunity for integrating optical devices at the vicinity of CMOS circuitry utilizing standard processes. Hence, leveraging CMOS integration technology has enabled large progress in demonstration of passive and active silicon nanophotonic devices such as wavelength division multiplexing, modulators, and switches, [1, 2].

However, integration of photodetectors requires materials that absorb light in the infrared. Germanium (Ge) is suitable due to its high absorption coefficient at 1.3 μ m and 1.5 μ m wavelengths; additionally, modification of standard CMOS processes will not be required because Ge is a front-end material used for gate strain engineering. Thus, compact waveguide-integrated Ge photodetectors can be fabricated simultaneously with amplifier circuits in order to make a receiver for an optical network. Nevertheless, the integration of Ge photodetector into the CMOS process flow is very challenging due to process complexity and severe temperature constraints. Front-end processes have a temperature budget of \sim 1000 $^{\circ}$ C, which is higher than the melting point of Ge. As a result, photodetectors fabricated only after completing high-temperature front-end processes have been demonstrated previously.

This paper presents experimental results obtained from an integration approach wherein Ge waveguide photodetectors have been fabricated in the front-end before the activation of CMOS well implants [3, 4]. By utilizing a lateral seeded crystallization method wherein the Ge waveguides are melted during high-temperature dopant activation, 30 μ m-long defect-free single-crystal

Ge-on-insulator waveguides were formed. This approach eliminates the need for selective epitaxial growth of Ge, and avoids high-density misfit dislocations formed due to lattice mismatch when growing Ge on Si substrate.

The cross-section TEM image in Fig. 1 illustrates the MSM photodetector after CMOS metallization steps have been completed. Interdigitated electrodes with separation of 200nm were utilized to achieve very high bandwidth. The photodetectors demonstrated with this integration approach operate at low applied bias voltages with bandwidth exceeding 40Gbps as shown by the open eye diagram in Fig. 2 [3, 4].

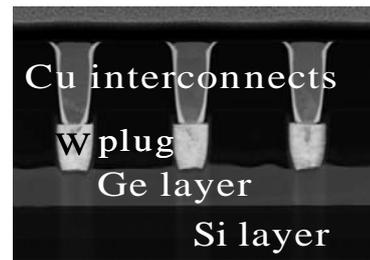


Fig. 1. Cross-section TEM image of a waveguide-integrated MSM germanium photodetector after completing metallization.

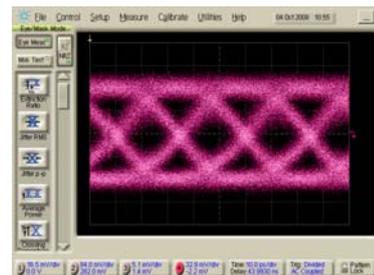


Fig. 2. 40Gbps eye diagram measured at 1.5V bias for 1.55 μ m light.

References

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