Economics and Design Challenges in Implementing CMOS Transimpedance Amplifers for 10Gb/s Operation

Ty Yoon, PhD
Basas Microelectronics, Beijiing 100083, China
Phone: +(86)13811530908, Email: tyyoon@basasmicro.com

Abstract ***This paper examines the technological challenges in implementing 10Gb/s Transimpedance Amplifiers in standard CMOS process technology. Circuit techniques for enabling 10Gb/s CMOS circuit operation are discussed. Paper concludes with measurements results for an actual 10Gb/s CMOS Transimpedance Amplifier.***

Introduction

Ever increasing internet network traffic, as well as high data rate multimedia contents such as HD video and high resolution photos are fueling the recent efforts to develop the next generation interconnect and network technologies such as 40/100GbE and Optical USB 3.0. Emergence of multi gigabit networks underscores the need for low cost, high performance components that can support 10Gb/s and above data rates. However, at 10Gb/s and beyond, the incumbent copper technology is too power hungry, and worse yet, lacks future scalability. Fiber technology appears to be a viable alternative, offering high performance and future proofing. For fiber technology to be cost competitive to copper, it is imperative that key interface ICs such as the Transimpedance Amplifier or TIA be manufactured using the lowest cost IC technology available. TIA is a critical component in the receive path, as its noise, gain, and frequency performance largely determine the overall data rate. This paper examines the design challenges in implementing a 10Gb/s TIA in a mature CMOS process. Several circuit techniques in overcoming CMOS device bandwidth limitation are described. Paper concludes with the actual measurement results for a 10Gb/s TIA fabricated in 0.18μm CMOS process.

Economics of CMOS Transimpedance Amplifier

CMOS technology has been the main driver for relentless technology scaling we have witnessed in the last several decades, also known as the Moore' Law. The beauty of CMOS technology and the fabless model is that the cost of building and maintaining a CMOS fab is shared across billions of ICs and hundreds of fabless semiconductor companies. Contrast this with a typical optical vendor, such as one for VCSEL or photodiode, who operates a small volume fab mainly to support its own in house product line. Then why has CMOS technology been unable to penetrate the market for optical interface ICs such as TIAs? Apart from technical challenges which will be discussed later, the main reason has been that the volume has not been large enough to fully exploit the cost savings and economies of scale that the CMOS technology commands. For instance, the market for 10Gb/s, driven mainly by backhaul telecom applications, has been on the order of millions [1]. In comparison, the market for CPUs, memory chips, and cellular ICs are on the order of billions. With the emergence of such large volume applications as 10GbE, Optical USB 3.0, the economics finally justify the deployment of CMOS technology for front-end optical interface applications[2]. Table 1 shows the cost per die as a function of expected number of units. Here CMOS is contrasted with InP HBT, which is one of the dominating technologies for 10Gb/s TIA markets. Typical numbers were assumed for mask NRE, wafer cost, and wafer size. Note testing and development costs are not included in the calculation. As can be seen, even for such a small volume as 1M, CMOS cost per die is much less than InP. As more blocks are integrated (ie, integrated TIA, LIA, and VCSEL Driver), the cost savings of CMOS will be even more dramatic. Another more subtle motivation for employing CMOS technology is that the supply domain for large volume datacom and consumer applications are dictated by CMOS ASICs, which typically run at 1.8V and below. Due to inherent limitation of large Vbe of InP and SiGe, these compount technologies will be unable to keep pace. In the future, as volume increases sufficiently for 40Gb/s market, performance of CMOS technology will be more than adequate, with CMOS at 45nm node offering Ft of 280GHz that is comparable to the fastest SiGe HBT available [3].

Technology	CMOS 0.18um	CMOS 0.13um	InP HBT
Cost per die/100k	$1.50	$2.50	$4.74
Cost per die/1M	$0.21	$0.29	$1.30
Cost per die/10M	$0.08	$0.06	$1.10

Table 1. TIA Die Cost as a Function of Number of Units

CMOS TIA Design Challenges

Simplified block diagram of a transimpedance amplifier is shown in Figure 2a. TIA is a feedback circuit whose small signal bandwidth is extended by the open loop gain Ao: BW = (1+Ao)/(Cin*Rf), where Cin is the photo diode capacitance Cpd plus the amplifier input

capacitance Cg, while Rf is the shunt feedback resistance. To achieve bandwidth of 10GHz for Cin = 0.3pF and Rf=500Ω, Ao has to be around 10. For good feedback margin, this gain has to be achieved with 3-dB bandwidth well in excess of 10GHz. Compared to InP or SiGe, CMOS device has lower transconductance and lower output impedance, rendering it extremely difficult to achieve gain of 10 (or 20dB) and 3-dB bandwidth of 10GHz with just a single gain stage.

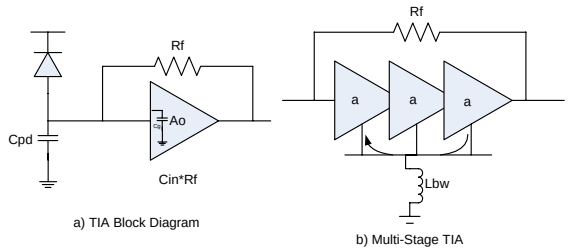

Figure 2 CMOS TIA Block Diagram

A solution is to cascade multiple stages, with each stage with much lower gain, but with much higher 3-dB bandwidth, as shown in Figure 2b. However, cascading multiple gain stages makes the TIA more susceptible to oscillation arising from the effect of power supply and gound bondwire inductance, since at 10GHz, the bondwire impedance becomes significant and cause parasitic feedback paths. A way to combat this problem is to adopt a differential topology. A penalty to be paid is higher input noise, since duplication of noise contributing devices causes 3dB higher input referred noise, leading to 1.5dB degradation in input optical sensitivity. However, this degradation can be compensated by migrating to a higher Ft CMOS process, and by employing innovative circuit techniques, where the effect of Cpd can be mitigated, thus leading to higher bandwidth and lower noise [4].

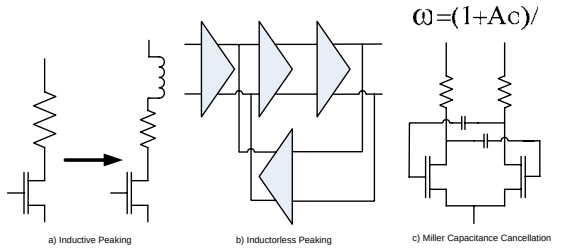

Figure 3. CMOS Bandwidth Enhancement Techniques

Inherehent bandwidth limitation of 0.18μm CMOS process can be overcome by various techniques as illustrated in Figure 3. The most widely used approach is the use of inductive peaking. Cascading an inductor in series with the resistive load device creates a zero in the amplifier's transfer function that boosts amplifier bandwidth at high frequencies. The drawback is the potentially large area on chip inductor can occupy. Recently, new embedded feedback techniques have been introduced that promise to provide the same bandwidth extension of inductors, but just using active devices, leading to lower chip area [5]. Inductless bandwidth extension techniques will be key as more TIAs are put in parallel for such array applications as 100GbE. Note that this technique appears to be a variant of Modified Cherry Hooper feedback technque that the author has introduced in a prior publication [6]. Another popular technique is to apply positive feedback across differential amplifier input and output in order to cancel out the effect of Miller capacitance [7].

0.18m CMOS TIA Test Results

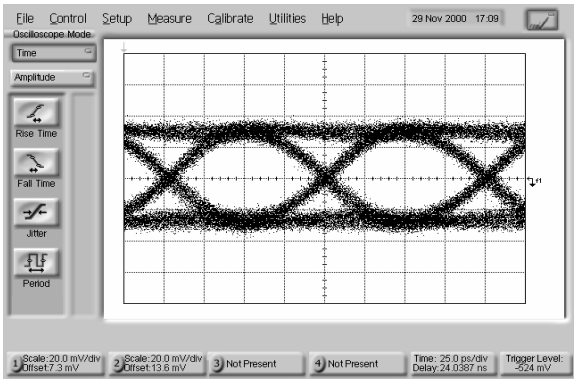

Figure 4. 0.18um CMOS TIA Eye Diagram at 10Gb/s

A differential CMOS TIA was implemented using TSMC 0.18um CMOS process. The amplifier uses inductive peaking and modified Cherry Hooper Feedback Architecture to achieve 9GHz bandwidth and 1.3Kohm of differential gain. Measured sensitivty at 10Gb/s is about -18dBm with photodiode capacitance of 0.15pF. Power dissipation was 60mA into 1.8V power supply. Figure 5 shows the measured eye diagram at -15dBm.

Conclusion

CMOS process has revolutionized the semiconductor industry with its remarkable technology scaling. It has also has become the dominant technology in commercial wireless markets, including WLAN and cellular, that were the dominion of compound semiconductor technologies only a decade ago. Now CMOS technology is poised to achieve similar economy of scale to enable ultra low cost, high performance fiber interface ICs, which will in turn trigger the emergence of optical fiber technology as the interface technology of choice for datacom as well as consumer applications.

References

1. 10G/40G/100G Infonetics Press Release, 2007
2. CIR, Data Comm. Tranceiver Markets Report, 2008
3. H. Li et al, VLSI Tech. Digest, p.56, June 2007
4. H. Kim et al, JSSC, vol.36, no.5, p.769. May 2001.
5. H. Huang et al, JSSC, vol.42, no.5, p.1111 May 2007
6. T. Yoon et al, VLSI Sym. Digest., p.188, June 1999
7. S. Galal et al JSSC, vol.38., no.12, Dec. 2003