Scalable quantum dot based optical interconnects

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Abstract
Scalable quantum dot based optical switches offer energy-efficient low-latency data routing. Low power penalty routing over multiple stages are feasible with with the prospect of larger scale photonic integration.

A pressing need for low-latency, high-bandwidth interconnection between high numbers of servers and communications channels has lead to renewed interest in high-connectivity, high-speed photonic circuits [1]. Tens of connections are required for emerging applications in server networks, with a future need for several hundreds in communications and high performance computing. However stringent energy- and cost- constraints are now guiding research.

The use of point to point optics in combination with massively parallel electronic switching imposes undesirable bottlenecks. Wavelength routing can impose an undesirable management complexity and an artificial constraint on the operating bandwidth of photonic elements. Semiconductor optical amplifier (SOA) switch technology offers fast nanosecond switching time, gain and a proven route to monolithic integration. Importantly, the broad multi-TeraHertz gain bandwidth also enables energy efficiency for multiplexed payloads without imposing constraints on data wavelength registration or modulation format. However, SOA based integrated circuits have so far only scaled to 4×4 connections, and a route-map to tens and hundreds of connections has so far been lacking.

Recent theoretical study has identified the possibility of energy efficient routing for 10×10Gb/s wavelength multiplexed payloads for several tens of connections. Here multi-stage networks used in electronic switching have been selected to suit the properties of semiconductor optical amplifier circuits [2]. The three stage Clos switch architecture is shown to enable good power penalty while optimally exploiting the intrinsic gain of the SOA switch elements. Base elements using a broadcast and switch architecture are able to advantageously balance a proportion of the gain against incurred losses without incurring excessive noise and distortion.

Quantum dot technology offers important advantages through low operating current operation, low noise, low distortion, and massive bandwidth [3]. More recently, the feasibility of high numbers of filter-free cascaded gates have been demonstrated [4]. This in turn has enabled the prospect of large scale switch fabrics implemented with cascades of smaller switching cells [5]. Recent research has explored the monolithic cascading and interconnection of such circuit elements on the same monolithic substrate [6]. Innovative crossbar switch architectures have been devised to facilitate compact integration with minimised numbers of electrodes [7]. The successful implementation of combiners, splitters, waveguide crossings and shuffle networks in the same quantum dot active medium has lead to new opportunities for larger scale integration.

Monolithic Multistage Architectures

A range of circuits have been devised and prototyped on five stack quantum dot active planes embedded in a InGaAsP separate confinement heterostructure. Three step etching with tailored photolithographic masks enable the deployment of shallow, deep and isolation waveguides throughout the circuit. These facilitate (i) low divergence waveguide crossings for low crosstalk crossovers, (ii) tight waveguide bends of down to 100 microns for ultracompact circuit layouts, and (iii) electronically isolated regions with isolation exceeding 10kΩ, all within the same circuits. Planarisation is performed prior to gold evaporation and plating. Devices are mounted as-cleaved, epoxy bonded to patterned ceramic tiles, and wire bonded. Figure 1 below shows an optical microscope image of an assembled circuit. Here two circuits are integrated on the same substrate. Wire bonds are visible connecting the gate and interconnection electrodes to individually addressable traces on a custom patterned ceramic tile.

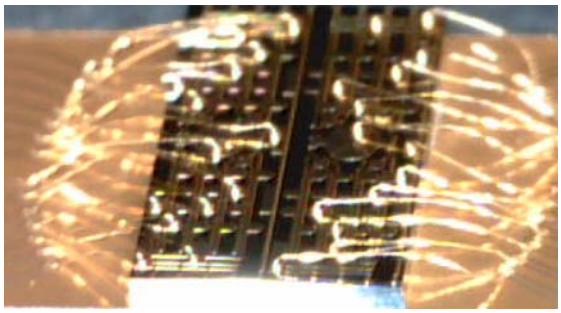

Fig. 1. Photograph of monolithic multi-stage switching circuits deployed in a quantum dot epitaxy. 4 input, 4 output circuits are shown wire bonded to a custom patterned ceramic test tile.

The scaling of such circuits to higher numbers of connections is predicated on the levels of signal degradation at each stage, and the possibility to provide the required interconnection between stages with low crosstalk and good power efficiency. Our studies have therefore focussed on the role of monolithic cascaded performance for circuit cells. Detailed comparisons between single and dual stage performance are presented in this work.

Routing with Quantum Dot Integrated Circuits

Two circuits are assessed. A single stage 2×2 crossbar switch circuit is compared with a dual stage 4×4 circuit. The assessment of data routing has been initially performed for 10Gb/s data with long pseudo-random bit sequences of 2^{31}-1 pattern length. Power penalty assessment is performed to identify contributions from the switch to signal degradation.

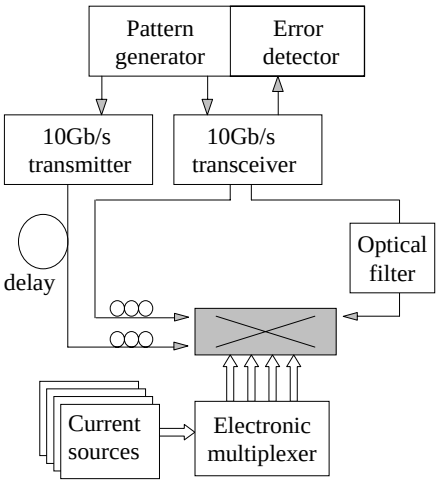

Fig. 2. Experimental arrangement for the assessment of switching circuits

Lensed fibres are scanned across both facets to characterise the switching paths. Currents into the switch electrodes are independently set. Input and output sections are biased at 160mA and 200mA for the single and dual stage circuits respectively. An additional 200mA is used for the central shuffle network in the dual stage switch. The gate currents are set to 120mA and 100mA for the single and dual stage circuits respectively. The output signal from the switch circuits is optically filtered for noise rejection and input to the 10 Gb/s transceiver to assess the bit error rate. No filtering is implemented within the integrated circuits themselves.

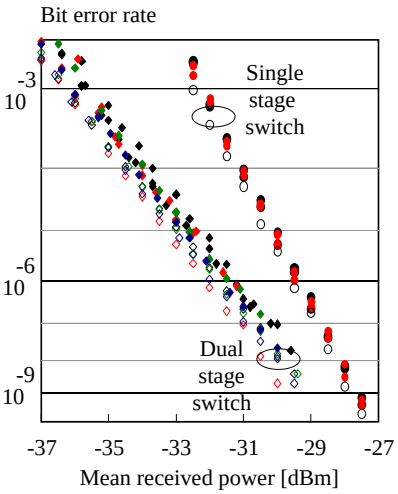

Fig. 3. Comparative bit error rate performance for single and dual stage monolithic switch networks

Power penalty performance is assessed from the bit error rate curves for both circuits to give path dependent power penalties of 0.15-0.25dB and 0.4-0.6dB for representative paths. This indicates a modest degradation in penalty with the increased number of integrated stages. The variation of power penalty for the measured range of paths is also observed to be low to within measurement error indicating little path dependence. The low values of power penalty are attributable to a modest level of amplified spontaneous emission and a high saturation observed under steady state operation. This is believed to be a direct consequence of the quantum dot gain medium. Dynamic routing is facilitated by direct electronic addressing of the amplifier gates. Ten concatonated pseudo random sequences are interleaved with 256ns duration guardbands to enable visibility for the 1.06us packets.

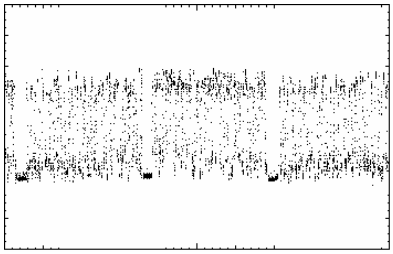

Fig. 4. Dynamic routing of 10Gb/s data in a dual stage monolithic switching circuit using a quantum dot epitaxy

Conclusions

A highly promising approach to enabling dynamic routing in highly scalable optoelectronic circuits has been identified. Very low power penalties of order 0.2dB/stage are observed in monolithic quantum dot circuits showing considerable promise for more complex monolithic interconnection networks.

References

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