

High-speed photonic signal processing for packet switching

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Abstract

Optical signal processing for packet switching is discussed. Starting from a packet switch architecture implementations of photonic building blocks are discussed.

Introduction

The routing of data packets for telecommunication is becoming a bottleneck because of severe requirements in speed and energy consumption. This development has brought discussions to what role optical packet switching can play in reducing the power of the network core routers [1]. The largest packet routers today are scalable to handle throughputs greater than 90 Terabit/s at the expense of power consumption greater than 1 Megawatt [2]. It is likely that such systems need to be scaled further in the future. This brings along significant challenges to overcome issues with respect to power consumption and heat-removal.

The most important advantage of using photonics in routers is that this makes opto-electronic conversion redundant. For example An OC-768 16:1 multiplexer/demultiplexer chipset typically dissipates 4.5 Watts of power [3]. An additional OC-48 8:1 multiplexer/demultiplexer typically dissipates 2.5 Watts of power [4]. This brings the total power consumption for the chipsets required to demultiplex a 40 Gb/s data stream into a 64 622 Mb/s data streams to approximately 45 Watts (per wavelength channel). An equal amount of power is required for multiplexing. Apart from that a 40 GHz clock recovery circuit typically dissipates 15 Watts of power [5]. This brings the total power consumption for demultiplexing, multiplexing and clock-recovery for a single 40 Gb/s channel in the order of 100 Watts. This sounds moderate, but in case of a thousand port switch this adds up to 100,000 watts of power, only for opto-electronic conversions. The existence of packet routers without opto-electronic conversion contributes significantly to the reduction of power in the system.

Parallelism and header processing

It is unlikely that an electronic Internet router architecture can be implemented in photonics and it is doubtful if it is useful trying this. On the other hand purely photonic router architectures potentially offer some advantages with respect to speed, latency, power-consumption and scalability. We focus on packet routers that have architectures as shown in Figure 1 (For reasons of simplicity, not all the interconnections are shown). At the inputs, WDM demultiplexers are used to separate the

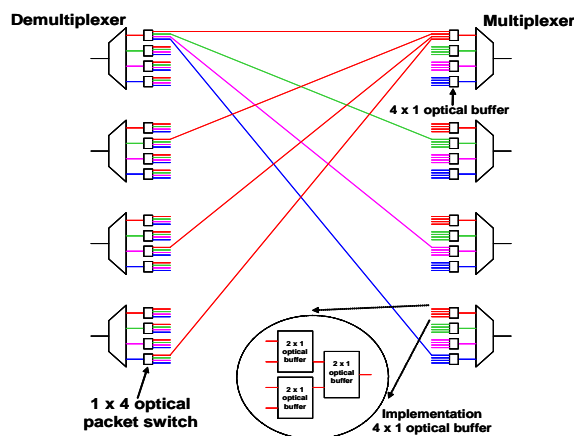


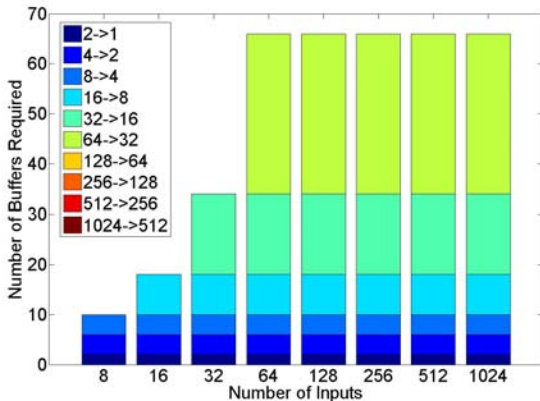
Figure 1: a typical optical packet switch architecture

WDM channels. As witnessed from Figure 1, such an cross-connect breaks down in two parts: a switching section and a “buffer-section” to resolve packet contention. The cross-connect shown in Figure 1 has only 4 input fibers each carrying 4 wavelength channels, but in the end, these cross connects need to be scaled to have many more input and output fibers, each carrying many more wavelength channels. In order to route data packets through such cross-connect while imposing sub-nanosecond latency the processing of the header is of key interest.

In our approach, we employ in-band labeling in combination with parallel optical header processing [6]. With this we mean that we encode the packet header with continuous wave signals with the duration of the packet pay-load. It is essential that the labels have wavelengths within the 20 dB spectral bandwidth of the payload. By using optical filters the labels can be separated from the payload. We treat the labels as binary information carriers. Thus the presence of 8 labels allows for addressing $2^8=256$ output ports. If we use N labels that are fed in a cascade of optical filters the header processor outputs a parallel N -bit word that contains the address information. The bits in the word are determined by in-band labels. This form of processing takes place “on-the-fly” and introduces very little latency. The output of the header processor can control a tunable laser to optically route the packets to the output. Alternatively, one can utilize an electronic recombinatory network to route the data to its destination. The use of space switches also makes such system transparent to bit-rate and data-format.

Micro-photonics for contention resolution

The second functionality in Figure 1 is a system to resolve contention resolution. Using standard queuing theory a worse case estimation can be made for the number of packets that have to be buffered as a function of the number of ports and the load. An example is given in Figure 2.



The graph presents the number of packets to be buffered in a cross-connect with the architecture presented in Figure 1, as a function of the number of ports for a load of 0.25 [7]. It can be observed that if the port number exceeds 64, 68 packets per output port need to be buffered. In the presentation, the role of micro-photonics for solving contention resolution is discussed.

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